REMARKS

Indication of Allowable Subject Matter

Applicant greatly appreciates the Examiner's allowance of claim 1-14, reflected in the Notice of Allowance mailed Jun. 28, 2007.

New Claim

Claim 15 has been newly added to further define and/or clarify the scope of the invention, in which the limitation introduced in claim 15 is comprised in the allowed claim 1.

Claim 15 states:

> 15. A survivor path decoding apparatus for a Viterbi decoder with a constraint length of *K*, comprising:
> ***a register-exchange network*** for receiving decision bits of states and generating decision vectors of survivor paths leading to said states at instant *i* according to said decision bits of said states from instant *i-L* to instant *i*, wherein said states are divided into said pairs of odd and even states, said decision vectors of said states are output every *L* iterations, and each of said decision vectors has a length of *L* bits; and
> a trace-back unit for storing said decision vectors of said states and finding a global survivor path sequence by following said decision vectors back from the best state at instant i-L, such that L decoded bits are output every L iterations.

(*Emphasis added*).

New claim 15 is allowable for at least the reason that the cited art taken alone or in-combination fails to teaches or suggest the claimed feature of "***a register-exchange network for receiving said decision bits of said*** 2^{K-1} ***states from said add-compare-select module and generating decision vectors of survivor paths leading***

to said 2^{K-1} ***states at instant i according to said decision bits of said*** 2^{K-1} ***states from instant i-L to instant i, wherein said decision vectors of said*** 2^{K-1} ***states are output every L iterations and each of said decision vectors has a length of L bits; and a trace-back unit for storing said decision vectors of said*** 2^{K-1} ***states and finding a global survivor path sequence by following said decision vectors back from the best state at instant i-L, such that L decoded bits are output every L iterations,***" as expressly-recited in new claim 15.

Azadet merely relevantly teaches a survivor memory unit to track the survivor paths. (see paragraph [0041], Azadet) Neither Azadet nor any cited reference teaches or suggests the limitation that "a register-exchange network for receiving **decision bits** of 2^{K-1} states and generating decision vectors of survivor paths leading to said 2^{K-1} states at instant i **according to said decision bits of said** 2^{K-1} **states from instant i-L to instant i**, said decision vectors of said 2^{K-1} states are **output every L iterations**, and **each of said decision vectors has a length of L bits**," as recited in new claim 15.

Further, the claimed embodiments can take advantage of the use of 2^{K-1} because "according to the invention, the trellis diagram for the rate 1/n encoder with a constraint length of K is organized in a butterfly structure." (see page, 10, lines 18-20). In addition, "the number of necessary ACS units is equal to half the number of total states, that is, $P=2^{k-2}$." (see p. 12, lines 9-11). Furthermore, none of the cited prior art references teaches that decision vectors of said 2^{K-1} states are **output every L iterations**, and **each of said decision vectors has a length of L bits** with the instant presented claimed structure.

For at least these reasons, new claim 15 patently defines over the cited art of record.

If, in the opinion of the Examiner, a telephonic conference would expedite the further examination and allowance of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,

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